CLAIMS

What is claimed is:

1.   A sync mark detector for identifying a sync mark in an incoming bitstream of a communications channel, comprising:

a bit comparing circuit that compares said sync mark bit-by-bit to said incoming bitstream if channel irregularities do not exist; and

a symbol comparing circuit that compares said sync mark symbol-by-symbol to said incoming bitstream if said channel irregularities do exist.

2.   The sync mark detector of claim 1 further comprising a front end that communicates with said bit and symbol comparing circuits, that outputs said incoming bitstream and that generates a channel irregularity signal when said channel irregularities exist.

3.   The sync mark detector of claim 1 further comprising a bit decision circuit that decodes said incoming bitstream.

4.   The sync mark detector of claim 3 further comprising a first buffer that communicates with said bit decision circuit and that stores M bits of said incoming bitstream at a desired phase.

5.   The sync mark detector of claim 3 further comprising a first post coding circuit that communicates with said bit decision circuit.

6.   The sync mark detector of claim 5 further comprising a first buffer that communicates with said first post coding circuit and that stores M bits of said incoming bitstream at a desired phase.

7.   The sync mark detector of claim 6 wherein said first post coding circuit performs INRZI post coding.

8.   The sync mark detector of claim 6 wherein said first post coding circuit performs NRZI post coding.

9.   The sync mark detector of claim 3 further comprising a second buffer that communicates with said bit decision circuit and that stores M bits of said incoming bitstream at a desired phase.

10.   The sync mark detector of claim 3 further comprising a second post coding circuit that communicates with said bit decision circuit.

11.   The sync mark detector of claim 10 further comprising a second buffer that communicates with said second post coding circuit and that stores M bits of said incoming bitstream at a desired phase.

12.   The sync mark detector of claim 10 wherein said second post coding circuit performs INRZI post coding.

13.   The sync mark detector of claim 10 wherein said second post coding circuit performs NRZI post coding.

14.   The sync mark detector of claim 1 wherein said bit comparing circuit implements a bit level matching rule.

15.   The sync mark detector of claim 1 wherein said symbol comparing circuit implements a symbol level matching rule.

16.   The sync mark detector of claim 14 wherein bit comparing circuit generates a sync mark found state when said bit level matching rule is satisfied.

17.   The sync mark detector of claim 15 wherein symbol comparing circuit generates a sync mark found state when said symbol level matching rule is satisfied.

18.   The sync mark detector of claim 1 wherein said sync mark in said incoming bitstream has large Hamming and symbol distances to provide low early alignment and low sync mark miss probabilities.

19.   The sync mark detector of claim 1 wherein a longest error event in said sync mark causes x bit errors and wherein a symbol length of said symbols in said incoming bitstream are limited to x-1.

20.   The sync mark detector of claim 1 wherein each symbol includes a plurality of bits.

21.   The sync mark detector of claim 1 wherein said sync mark includes (4+3s) symbols and said symbol comparing circuit implements a (2+s) out of (4+3s) symbol matching rule for identifying sync marks.

22.   The sync mark detector of claim 1 wherein said communications channel is a disk drive.

23.   The sync mark detector of claim 1 wherein said sync mark does not contain "101" or "010" bits and does not contain "10001" or "01110" patterns starting immediately before a symbol boundary.

24.   The sync mark detector of claim 14 wherein said bit level matching rule is met if bit differences are less than half of the Hamming distance d_H.

25.   The sync mark detector of claim 14 wherein said bit level matching rule is met if bit differences are greater than or equal to $M - [(d_H - 1)/2]$.

26.   The sync mark detector of claim 1 wherein said channel irregularities produce long consecutive bit errors and wherein said channel irregularities are caused by at least one of thermal asperity and media defects.

27.   The sync mark detector of claim 1 wherein said sync mark detector is implemented in software and is executed by a processor and memory.

28.   The sync mark detector of claim 17 wherein said symbol matching rule allows an error event to produce more that one symbol error.

29.   A sync mark detector for identifying a sync mark in an incoming bitstream of a communications channel, comprising:

bit comparing means for comparing said sync mark bit-by-bit to said incoming bitstream if channel irregularities do not exist; and

symbol comparing means for comparing said sync mark symbol-by-symbol to said incoming bitstream if said channel irregularities do exist.

30.   The sync mark detector of claim 29 further comprising front end means for communicating with said bit and symbol comparing means, for providing said incoming bitstream and for generating a channel irregularity signal when said channel irregularities exist.

31.   The sync mark detector of claim 29 further comprising bit decision means for decoding said incoming bitstream.

32.   The sync mark detector of claim 31 further comprising first buffer means for communicating with said bit decision means and for storing M bits of said incoming bitstream at a desired phase.

33.   The sync mark detector of claim 31 further comprising a first post coding means for coding said incoming bitstream.

34.   The sync mark detector of claim 33 further comprising first buffer means for communicating with said first post coding means and for storing M bits of said incoming bitstream at a desired phase.

35.   The sync mark detector of claim 34 wherein said first post coding means performs INRZI post coding.

36.   The sync mark detector of claim 34 wherein said first post coding means performs NRZI post coding.

37.   The sync mark detector of claim 31 further comprising second buffer means for communicating with said bit decision means and for storing M bits of said incoming bitstream at a desired phase.

38.   The sync mark detector of claim 31 further comprising second post coding means for communicating with said bit decision means.

39.   The sync mark detector of claim 38 further comprising second buffer means for communicating with said second post coding means and for storing M bits of said incoming bitstream at a desired phase.

40.   The sync mark detector of claim 38 wherein said second post coding means performs INRZI post coding.

41.   The sync mark detector of claim 38 wherein said second post coding means performs NRZI post coding.

42.   The sync mark detector of claim 29 wherein said bit comparing means implements a bit level matching rule.

43.   The sync mark detector of claim 29 wherein said symbol comparing means implements a symbol level matching rule.

44.   The sync mark detector of claim 42 wherein bit comparing means generates a sync mark found state when said bit level matching rule is satisfied.

45.   The sync mark detector of claim 43 wherein symbol comparing means generates a sync mark found state when said symbol level matching rule is satisfied.

46.   The sync mark detector of claim 29 wherein said sync mark in said incoming bitstream has large Hamming and symbol distances to provide low early alignment and low sync mark miss probabilities.

47.   The sync mark detector of claim 29 wherein a longest error event in said sync mark causes x bit errors and wherein a symbol length of said symbols in said incoming bitstream are limited to x-1.

48.   The sync mark detector of claim 29 wherein each symbol includes a plurality of bits.

49.   The sync mark detector of claim 29 wherein said sync mark includes (4+3s) symbols and said symbol comparing means implements a (2+s) out of (4+3s) symbol matching rule for identifying sync marks.

50.   The sync mark detector of claim 29 wherein said communications channel is a disk drive.

51.   The sync mark detector of claim 29 wherein said sync mark does not contain "101" or "010" bits.

52.   The sync mark detector of claim 29 wherein said sync mark does not contain "10001" or "01110" patterns starting immediately before a symbol boundary.

53.   The sync mark detector of claim 42 wherein said bit level matching rule is met if bit differences are less than half of the Hamming distance d_H.

54.   The sync mark detector of claim 42 wherein said bit level matching rule is met if bit differences are greater than or equal to $M - [(d_H - 1)/2]$.

55.   The sync mark detector of claim 29 wherein said channel irregularities cause long consecutive bit errors.

56.   The sync mark detector of claim 29 wherein said channel irregularities are caused by at least one of thermal asperity and media defects.

57.   The sync mark detector of claim 29 wherein said sync mark detector is implemented in software and is executed by a processor and memory.

58.   A method for identifying a sync mark in an incoming bitstream of a communications channel, comprising:

comparing said sync mark bit-by-bit to said incoming bitstream if channel irregularities do not exist; and

comparing said sync mark symbol-by-symbol to said incoming bitstream if said channel irregularities do exist.

59.   The method of claim 58 further comprising generating a channel irregularity signal when said channel irregularities exist.

60.   The method of claim 58 further comprising decoding said incoming bitstream.

61.   The method of claim 60 further comprising storing M bits of said incoming bitstream at a desired phase.

62.   The method of claim 60 further comprising post coding said incoming bitstream using a first post coding method.

63.   The method of claim 62 further comprising storing M bits of said incoming bitstream at a desired phase.

64.   The method of claim 62 wherein said first post coding method is INRZI post coding.

65.   The method of claim 62 wherein said first post coding method is NRZI post coding.

66.   The method of claim 60 further comprising storing M bits of said incoming bitstream at a desired phase.

67.   The method of claim 60 further comprising post coding said incoming bitstream using a second post coding method.

68.   The method of claim 67 further comprising storing M bits of said incoming bitstream at a desired phase.

69.   The method of claim 67 wherein said second post coding method is INRZI post coding.

70.   The method of claim 67 wherein said second post coding method is NRZI post coding.

71.   The method of claim 58 further comprising implementing a bit level matching rule.

72.   The method of claim 58 further comprising implementing a symbol level matching rule.

73.   The method of claim 71 further comprising generating a sync mark found state when said bit level matching rule is satisfied.

74.   The method of claim 72 further comprising generating a sync mark found state when said symbol level matching rule is satisfied.

75.   The method of claim 58 wherein said sync mark in said incoming bitstream has large Hamming and symbol distances to provide low early alignment and low sync mark miss probabilities.

76.   The method of claim 58 wherein a longest error event in said sync mark causes x bit errors and wherein a symbol length of said symbols in said incoming bitstream are limited to x-1.

77.   The method of claim 58 wherein each symbol includes a plurality of bits.

78.   The method of claim 58 wherein said sync mark includes (4+3s) symbols and said symbol matching rule is a (2+s) out of (4+3s) for identifying sync marks.

79.   The method of claim 58 wherein said communications channel is a disk drive.

80.   The method of claim 58 wherein said sync mark does not contain "101" or "010" bits.

81.   The method of claim 58 wherein said sync mark does not contain "10001" or "01110" patterns starting immediately before a symbol boundary.

82.   The method of claim 71 wherein said bit level matching rule is met if bit differences are less than half of the Hamming distance d_H.

83.   The method of claim 71 wherein said bit level matching rule is met if bit differences are greater than or equal to $M - [(d_H - 1)/2]$.

84.   The method of claim 58 wherein said channel irregularities cause long consecutive bit errors.

85.   The method of claim 58 wherein said channel irregularities are caused by at least one of thermal asperity and media defects.

86.   The method of claim 29 wherein said method is implemented in software and is executed by a processor and memory.